In the Specification:

Please insert the following paragraphs below at page 4, after line 6:

FIG. 5 is a semiconductor die undergoing analysis, according to another example embodiment of the present invention;

FIG. 6 is the semiconductor die of FIG. 5 undergoing further analysis, according to another example embodiment of the present invention;

Please amend the paragraph at page 4, lines 7-8, as indicated below.

FIG. [[5]]7 is a system for analyzing a semiconductor die, according to another example embodiment of the present invention.

Please amend the paragraph at page 6, lines 6-14 as indicated below.

In one particular implementation, the present invention is used in connection with defect analysis and identification methods used to identify a defective resistive interconnect. Resistive interconnects are often developed as a result of a void in conductive material used for the interconnect. For an example manner in which to identify a resistive interconnect, reference may be made to U.S. Patent Application Serial No. 09/586,518 (AMDA.455PA/TT3843), entitled "Resistivity Analysis" and filed on June [[6]]2, 2000, which is incorporated herein by reference. Once a resistive interconnect is identified, the interconnect is accessed and imaged in a manner not inconsistent with the various example embodiments described herein.